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PTO/SB/21 (10-96)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/787,116
Filing Date	Feb. 27, 2004
First Named Inventor	Tadahiko HISANO
Group Art Unit	2182
Examiner Name	Rehana Perveen
Total Number of Pages in This Submission: 14	Attorney Docket Number

ENCLOSURES *(check all that apply)*

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition Checklist and Accompanying Petition
- [ ] To Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group (*Appeal Notice, Brief, Reply Brief*)
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Additional Enclosure(s) *(please identify below)*:

Petition for Requesting Certificate of Correction of Patent No. 6952,742

Remarks

Certificate NOV 25 2005 of Correction

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Tadahiko Hisano
Signature	Tadahiko Hisano
Date	November 16, 2005

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on this date:

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NOV 28 2005

OIPE IAP55 NOV 22 2005 PATENT & TRADEMARK OFFICE

Patent No.: 6,952,742 B2

Date of Patent: Oct. 4, 2005

Inventor: Tadahiko HISANO

For: EXTERNAL STORAGE DEVICE AND METHOD OF ACCESSING SAME

Petition for Requesting Certificate of Correction under 37 CFR 1.322

Commissioner of Patents and Trademarks,

Washington, D.C. 20231

Sir,

Patentee (Inventer) hereby submits Petition for Requesting Certificate Correction to correct mistakes of Front page, claim 11 (column 28 at line 49 to 51), and claim 27 (column 30 at line 8 to 16).

In Front page, the front page view should appear as Fig. 19 as to correspond to the "application data sheet" filed with the above application as attached sheet of page 1 line 11, column of "Suggested Drawing Figure".

Claim 11 (column 28 at line 49 to 51) and claim 27 (column 30 at line 8 to 16) have clerical mistakes that is "misquoting claim number" and sholuld be corrected as to correspond to the amended claims filed on Oct. 25 2005 (mailed on Oct. 21 2004) as attached sheet "resubmission of amendment of claims" of page 2 line 15 to 16 (in which it is shown as claim 12) and page line 30 to page 5 line 3 (in which it is shown as claim 29)

Those mistakes seem to be on the part of the Patent and Trademark Office, so that due fee will not be required. And should it is believed to be certificate correction of above mistakes.

Respectfully submitted,

Tadahiko Hisano

Signature: Tadahiko Hisano

Date : Nov. 10, 2005

NOV 28 2005

Attachment:

2 sheets of "Certificate of Correction"
7 sheets of print-out of "resubmission of amendment of claims" downloaded from the PAIR page of the above application
2 sheets of print-out of "application data sheet" downloaded from the PAIR page of the above application

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NOV 2 8 2005

OIPE IAP55 NOV 22 2005 PATENT & TRADEMARK OFFICE

Application Data Sheet

Application Information

Application Type::	Regular
Subject Matter::	Utility
Suggested Classification::	710/3; 710/4; 710/20; 710/21;710/23; 710/33
Suggested Group Art Unit::	2182
CD-ROM or CD-R?	None
Title::	EXTERNAL STORAGE DEVICE AND METHOD OF ACCESSING SAME
Request for Early Publication?::	No
Request for Non-Publication?::	No
Suggested Drawing Figure::	19
Total Drawing Sheets::	25
Small Entity::	Yes
Petition included?::	No
Secrecy Order in Parent Appl.?::	No

Domestic Priority Information

Application::	Continuity Type:	Parent Application::	Parent Filing Date::
This Application	Division of	10/197.479	07/18/2002
10/197.479	An application claiming the benefit under 35 USC 119	09/644,650	08/24/2000
09/644,650	An application claiming the benefit under 35 USC 119	08/913,170	09/05/1997
08/913,170	An application claiming the benefit under 35 USC 119 and/or § 365(b)	PCT/JP96/00519	03/05/1996

Foreign Priority Information

Country::	Application Number::	Filing Date::	Priority Claimed::
Japan	7-70452	03/06/1995	Yes
Japan	7-231975	08/16/1995	Yes
Japan	7-279866	10/04/1995	Yes

The certified copy was filed in prior Application PCT/JP96/00519.

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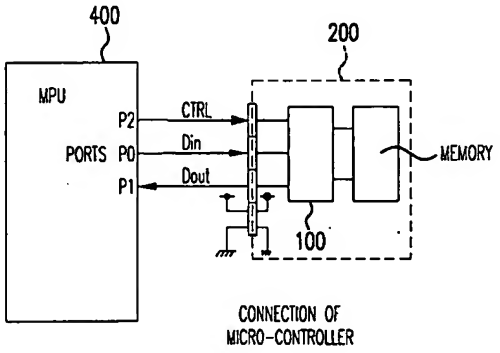
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,952,742 B2
DATED : October 4, 2005
INVENTOR(S) : Tadahiko HISANO

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Frontpage, the Frontpage view should appear as follows:



MAILING ADDRESS OF SENDER:
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PATENT NO. 6,952,742

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,952,742 B2
DATED : October 4, 2005
INVENTOR(S) : Tadahiko HISANO

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Claim 11 (in column 28 at line 49 to 51) should apper as follows:

11. The storage device according to claim 10, further comprising, a switch connected to the port for setting the status.

Claim 27 (column 30 at line 8 to 16) should apper as follows:

27. The apparatus according to claim 26, wherein the storage device inputs a command from the data input, provides the data to the memory in accordance with the command to store the data in the memory or to output data in the memory to the data output, and the apparatus provides the control signal to the control input from the interface, and the command and the data to the data input from the interface, to store the data in the memory or to output data in the memory to the data output.

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PATENT NO. 6,952,742

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OCT 25 2004
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AMENDMENTS TO CLAIMS

Claims 1, 4, 9, 19, 22, 23, 28 and 31 are amended,
Claims 3, 21, and 30 are canceled, and
Claims 39-42 are added.
Please replace prior claims to the following listing of the amended claims:

1. (Currently Amended) A storage device comprising:
a memory for storing data ;and
a circuit having a data input, a control input, and a data output;
wherein ~~the circuit provides data input from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input in the memory or to output data stored in the memory to the data output~~ the circuit provides an address input from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input at the address in the memory or to output data at the address in the memory to the data output.

2. (Original) The storage device according to claim 1, wherein the circuit inputs a command from the data input to the memory in accordance with the control signal to store the data in the memory or to output data stored in the memory to the data output.

3.(Canceled)

4. (Currently Amended) The storage device according to claim ~~3~~1, wherein the circuit has ports for providing the data and the address to the memory and a data bus for transferring the data from the data input to one of the ports by the control signal of the control input.

5. (Original) The storage device according to claim 4, wherein the circuit has another data bus for transferring the data from the one of the ports to the data output by the control signal.

6. (Original) The storage device according to claim 4, wherein the ports comprise flip-flops for holding and outputting the data from the data bus to the memory by the control signal, and buffers for outputting the data from the memory to the data bus by the control signal.

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7. (Original) The storage device according to claim 4, wherein selection and read/write of the ports is controlled by bits input to the control input.

8. (Original) The storage device according to claim 4, wherein the circuit inputs a command for selection and read/write of the ports from the data input by the control signal of the control input.

9. (Currently Amended) The storage device according to claim ~~3~~1, wherein the circuit inputs part of the address from the data input to set the part to selected bit of a held address that is modified by the part, and provides the modified address to the memory.

10. (Original) The storage device according to claim 1, wherein the circuit inputs part of the data from the data input to set the part to selected bit of held data that is modified by the part, and provides the modified data to the memory.

11. (Original) The storage device according to claim 1, wherein the circuit has a readable port set to a status for identification and control of access to the memory.

12. (Original) The storage device according to claim 11, further comprising, a switch connected to the port for setting the status.

13. (Original) The storage device according to claim 1, further comprising, another memory for storing data to which the circuit provides the data.

14. (Original) The storage device according to claim 1, wherein data for identification in a predetermined header area is written in the memory.

15. (Original) The storage device according to claim 1, wherein the memory has a mode in which the data are successively output from the memory.

16. (Original) The storage device according to claim 1, wherein the memory is one of a ROM, a static memory, an EEPROM, a dynamic memory, a flash memory, and a ferroelectics memory.

17. (Original) The storage device according to claim 1, wherein the data input inputs parallel data and the data output outputs parallel data.

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18. (Original) The storage device according to claim 1, further comprising, a connector connected to the data input, the data output, and the control input, and for supplying power to the storage device.

19. (Currently Amended) A method for access to a storage device having a data input, a control input, a data output, and a memory for storing data, wherein ~~the storage device inputs data from the data input, and provides the data to the memory in accordance with a control signal from the control input to store the data in the memory~~ the storage device provides an address from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input at the provided address in the memory or to output data at the address in the memory to the data output, comprising:

providing an address to the data input to output the address to the memory;

providing data to the data input to output the data to the memory; and

providing a first control signal to the control input to store the data at the address into the memory.

20. (Original) The method according to claim 19, wherein the storage device inputs a command from the data input, and provides the data to the memory in accordance with the command to store the data in the memory or to output data in the memory to the data output, comprising:

providing the command to the data input;

providing data to the data input to output the data to the memory; and

providing the first control signal to the control input to store the data into the memory in accordance with the command.

21.(Canceled)

22. (Currently Amended) The method according to claim ~~21~~19, further comprising:

providing an address to the data input to set the address of memory; and

providing a second control signal to the control input to output the data at the address in the memory to the data output.

23. (Currently Amended) The method according to claim ~~21~~19, further comprising, providing part of the address to set the part to selected bits of an address

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held in the storage device for modifying the address and output the modified address to the memory.

24. (Original) The method according to claim 19, wherein the data output outputs the data transfered between the data input and the memory, comprising:

inputting the transferred data from the data output to confirm whether the data is correct.

25. (Original) The method according to claim 19, wherein the memory has a mode in which the data are successively output from the memory, and the method further comprises turning control status of the memory by providing signals to the storage device such that the memory operates in the mode.

26. (Original) The method according to claim 19, wherein the storage device has a readable port set to a status for identification of an access type of the memory, comprising, reading the status to identify access type of the memory.

27. (Original) The method according to claim 19, wherein the data input inputs parallel data and the data output outputs parallel data.

28. (Currently Amended) An apparatus having (1) an interface for data exchange from and to a storage device having a data input, a control input, a data output, and a memory for storing data, wherein ~~the storage device inputs data from the data input, provides the data to the memory in accordance with a control signal from the control input to store the data memory~~ the storage device provides an address from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input at the provided address in the memory or to output data at the address in the memory to the data output, and (2) a connector for connecting the data input, a data output and the control input to the interface and supplying power to the storage device, wherein the apparatus provides the control signal to the control input from the interface, and the data or an address to the data input from the interface to store the data at the address in the memory or to output data at the address in the memory to the data output.

29. (Original) The apparatus according to claim 28, wherein the storage device inputs a command from the data input, provides the data to the memory in accordance with the command to store the data in the memory or to output data in the memory to

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the data output, and the apparatus provides the control signal to the control input from the interface, and the command and the data to the data input from the interface, to store the data in the memory or to output data in the memory to the data output.

30.(Canceled)

31. (Currently Amended) The apparatus according to claim ~~30~~28, wherein the apparatus provides part of the address to the data input to set the part to selected bits of an address held in the storage device for modifying the address and output the modified address to the memory.

32. (Original) The apparatus according to claim 28, wherein the memory has a mode in which the data are successively output from the memory, and the apparatus provides signals to the storage device such that the memory operates in the mode by turning control status of the memory.

33. (Original) The apparatus according to claim 28, wherein the apparatus exchanges data among a plurality of the storage devices, through the interface, and the apparatus further comprises connectors for connecting the data inputs of the storage devices to the interface and connecting the data inputs to each other.

34. (Original) The apparatus according to claim 28, wherein the data output outputs data transferred between the data input and the memory, and the apparatus inputs the transferred data from the data output to confirm whether the data is correct.

35. (Original) The apparatus according to claim 28, wherein the storage device has a readable port set to a status for identification and control of access to the memory, and the apparatus reads the status from the interface to identify access type of the memory.

36. (Original) The apparatus according to claim 28, wherein supplying power to the storage device is controlled.

37. (Original) The apparatus according to claim 28, wherein the data input inputs parallel data which the interface provides to the data input and the data output outputs parallel data which the interface inputs from the data output.

38. (Original) The apparatus according to claim 28, further comprising, a microcontroller in which the interface is provided.

39. (New) An apparatus having (1) an interface for data exchange from and to the external storage device having a data input, a data output, a control input, and a memory provided an address from the data input in accordance with a control signal from the control input to output data at the provided address in the memory from the data output, and (2) a connector for connecting the data input, a data output and the control input to the interface and supplying power to the external storage device, wherein the apparatus provides the control signal to the control input, and changed part of the address to the data input from the interface to set the part to selected bits of the address held in the external storage device for modifying the address so that the external storage device outputs the data stored at the modified address in the memory from the data output.

40. (New) An apparatus having (1) an interface for data exchange from and to the external storage device having a data input, a data output, a control input, and a memory provided an address from the data input in accordance with a control signal from the control input to output data at the provided address in the memory from the data output, wherein the memory has a mode in which the data are successively output from the memory, and (2) a connector for connecting the data input and the control input to the interface and supplying power to the external storage device, wherein the apparatus provides the control signal to the control input, and the address to the data input from the interface to output data at the address in the memory from the data output, and sets a value into the interface to turn control status of the memory such that the memory operates in the mode.

41. (New) An apparatus having (1) an interface for data exchange from and to the external storage device having a data input, a data output, a control input, and a memory provided an address from the data input in accordance with a control signal from the control input to output data at the provided address in the memory from the data output, and a readable port set to a status for identification and control of access to the memory, and (2) a connector for connecting the data input and the control input to the interface and supplying power to the external storage device, wherein the apparatus reads the status from the interface to identify access of the memory, and provides the control signal to the control input, and the address to the data input from the interface to output the data at the address in the memory from the data output.

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42. (New) An apparatus having (1) an interface for data exchange from and to a storage device having a data input, a control input, a data output, and a memory for storing data, wherein the storage device inputs a command from the data input in accordance with a control signal from the control input to output data in the memory from the data output, and (2) a connector for connecting the data input, a data output and the control input to the interface and supplying power to the storage device, wherein the apparatus provides the control signal to the control input from the interface, and the command to the data input from the interface to output data in the memory from the data output.

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